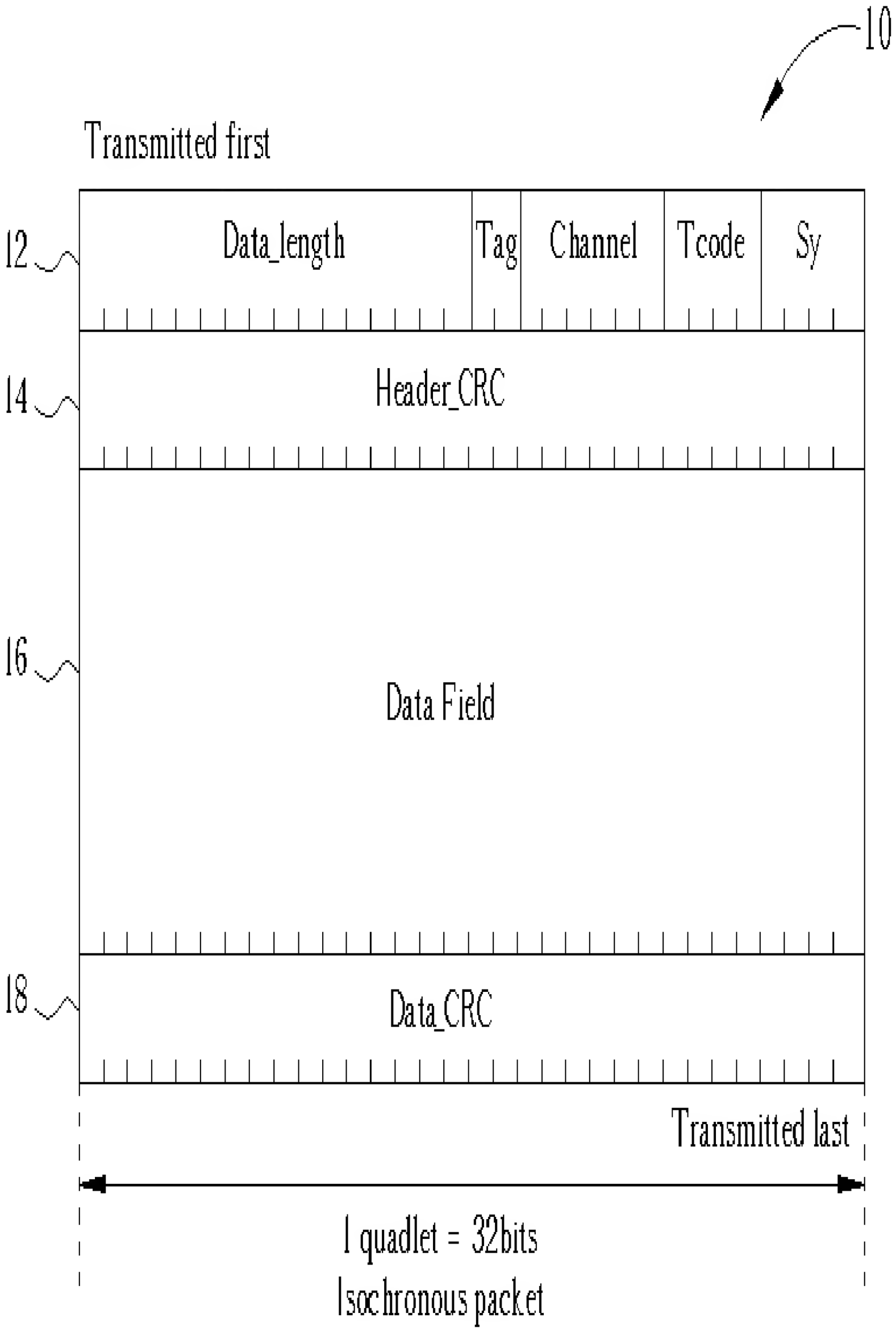

Fig. 1 Prior art

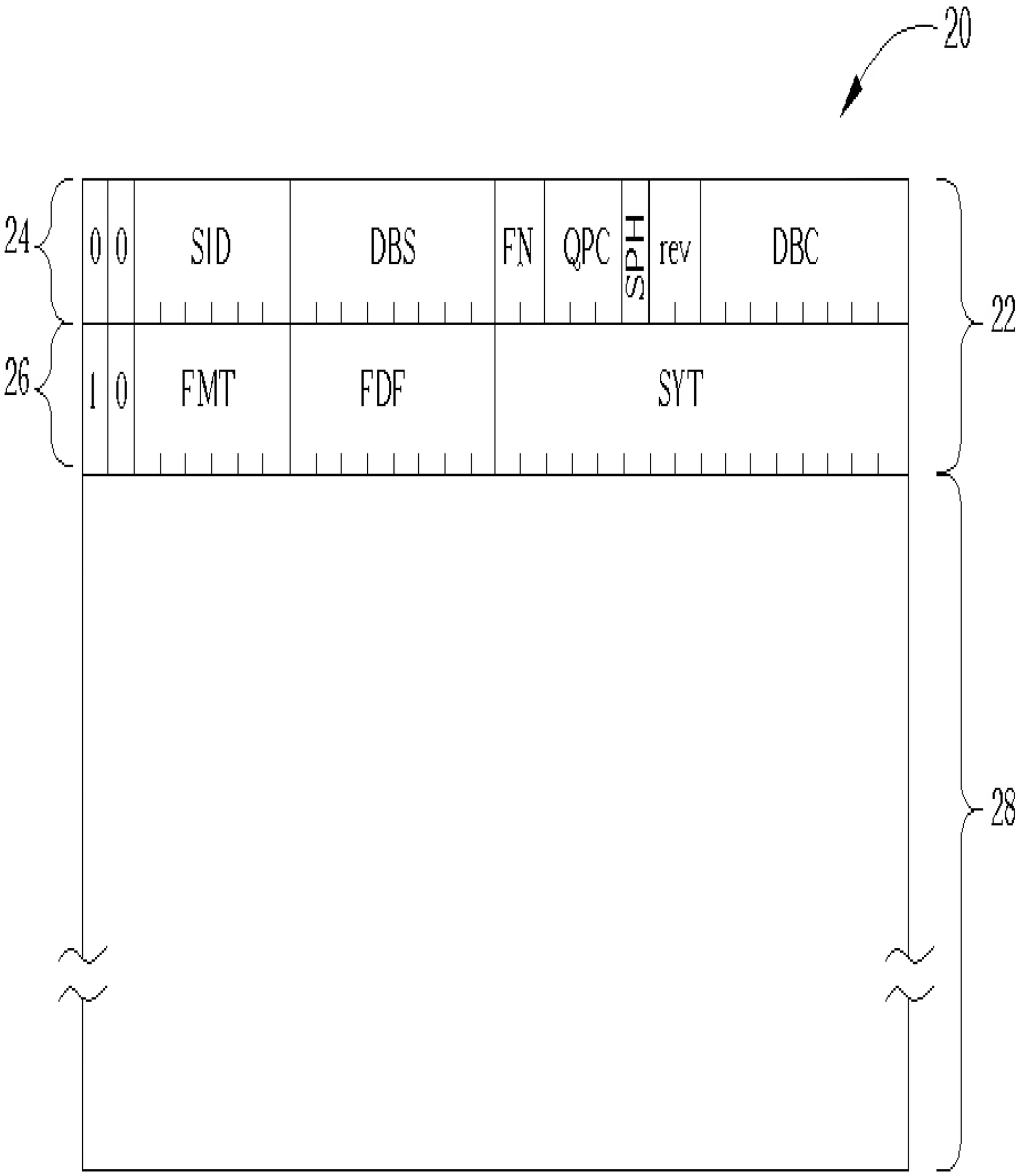

Fig. 2 Prior art

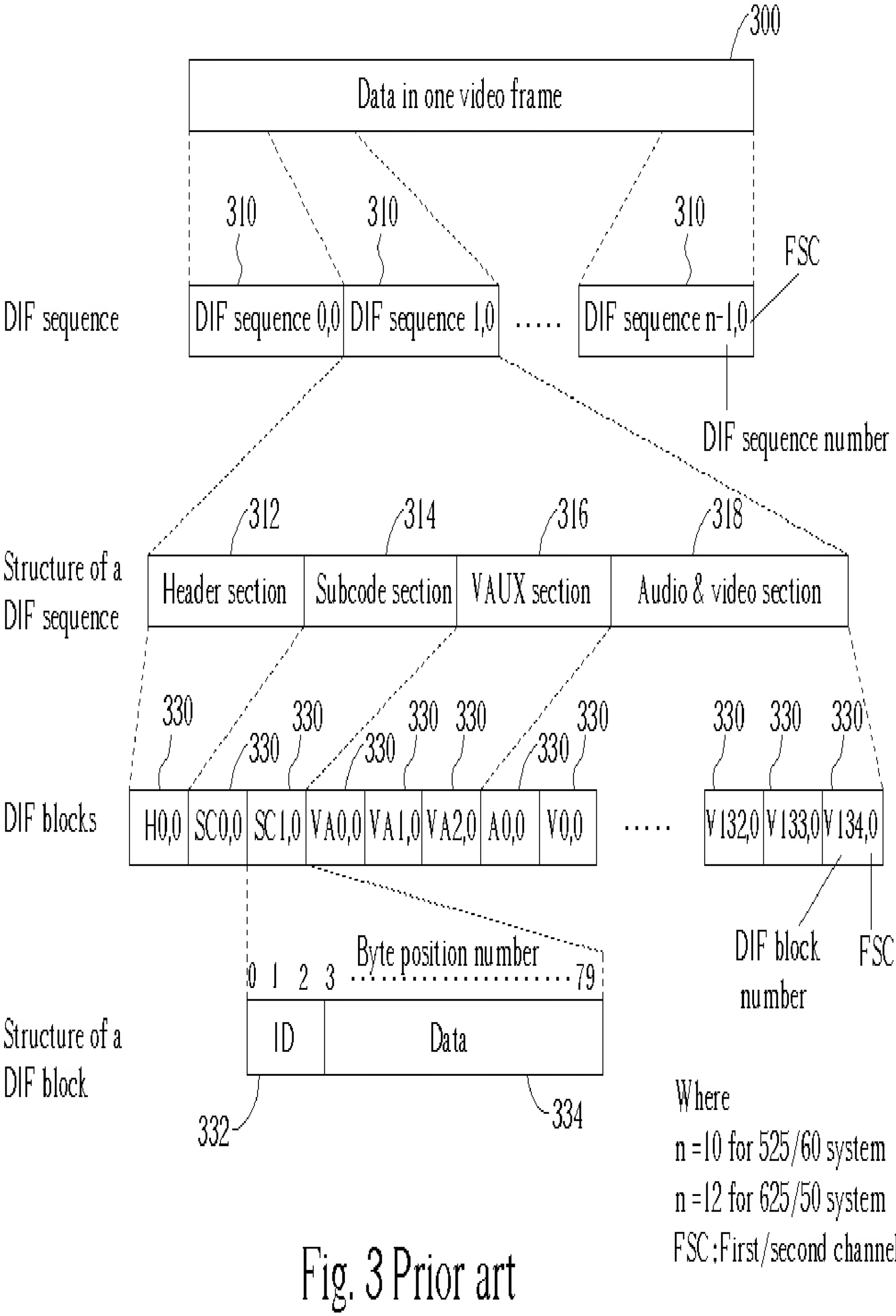

Fig. 3 Prior art

DIF blocks

H0,i	SC0,i	SC1,i	VA0,i	VA1,i	VA2,i

A0,i	V0,i	V1,i	V2,i	V3,i	V4,i	V5,i	V6,i	V7,i	V8,i	V9,i	V10,i	V11,i	V12,i	V13,i	V14,i

A1,i	V15,i	V16,i	V17,i	V18,i	V19,i	V20,i	V21,i	V22,i	V23,i	V24,i	V25,i	V26,i	V27,i	V28,i	V29,i

A2,i	V30,i	V31,i	V32,i	V33,i	V34,i	V35,i	V36,i	V37,i	V38,i	V39,i	V40,i	V41,i	V42,i	V43,i	V44,i

A3,i	V45,i	V46,i	V47,i	V48,i	V49,i	V50,i	V51,i	V52,i	V53,i	V54,i	V55,i	V56,i	V57,i	V58,i	V59,i

A4,i	V60,i	V61,i	V62,i	V63,i	V64,i	V65,i	V66,i	V67,i	V68,i	V69,i	V70,i	V71,i	V72,i	V73,i	V74,i

A5,i	V75,i	V76,i	V77,i	V78,i	V79,i	V80,i	V81,i	V82,i	V83,i	V84,i	V85,i	V86,i	V87,i	V88,i	V89,i

A6,i	V90,i	V91,i	V92,i	V93,i	V94,i	V95,i	V96,i	V97,i	V98,i	V99,i	V100,i	V101,i	V102,i	V103,i	V104,i

A7,i	V105,i	V106,i	V107,i	V108,i	V109,i	V110,i	V111,i	V112,i	V113,i	V114,i	V115,i	V116,i	V117,i	V118,i	V119,i

A8,i	V120,i	V121,i	V122,i	V123,i	V124,i	V125,i	V126,i	V127,i	V128,i	V129,i	V130,i	V131,i	V132,i	V133,i	V134,i

DIF block number

Where

i ;FSC

i=0 for 25 Mb/s structure

i=0,1 for 50 Mb/s structure

H0,i ;DIF block in header section

SC0,i to SC1,i ;DIF blocks in subcode section

VA0,i to VA2,i ;DIF blocks in VAUX section

A0,i to A8,i ;DIF blocks in audio section

V0,i to V134,i ;DIF blocks in video section

Fig. 4 Prior art

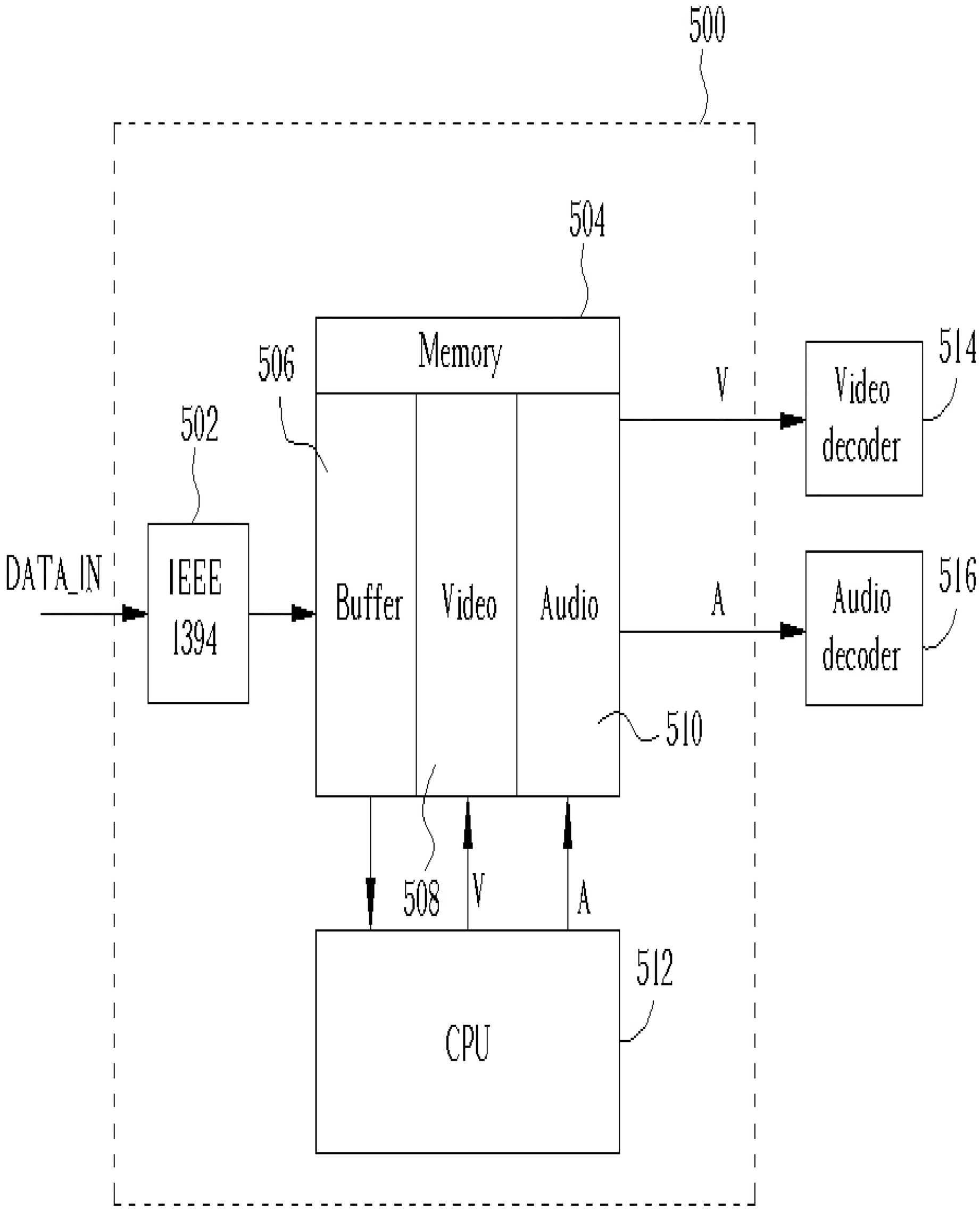

Fig. 5 Prior art

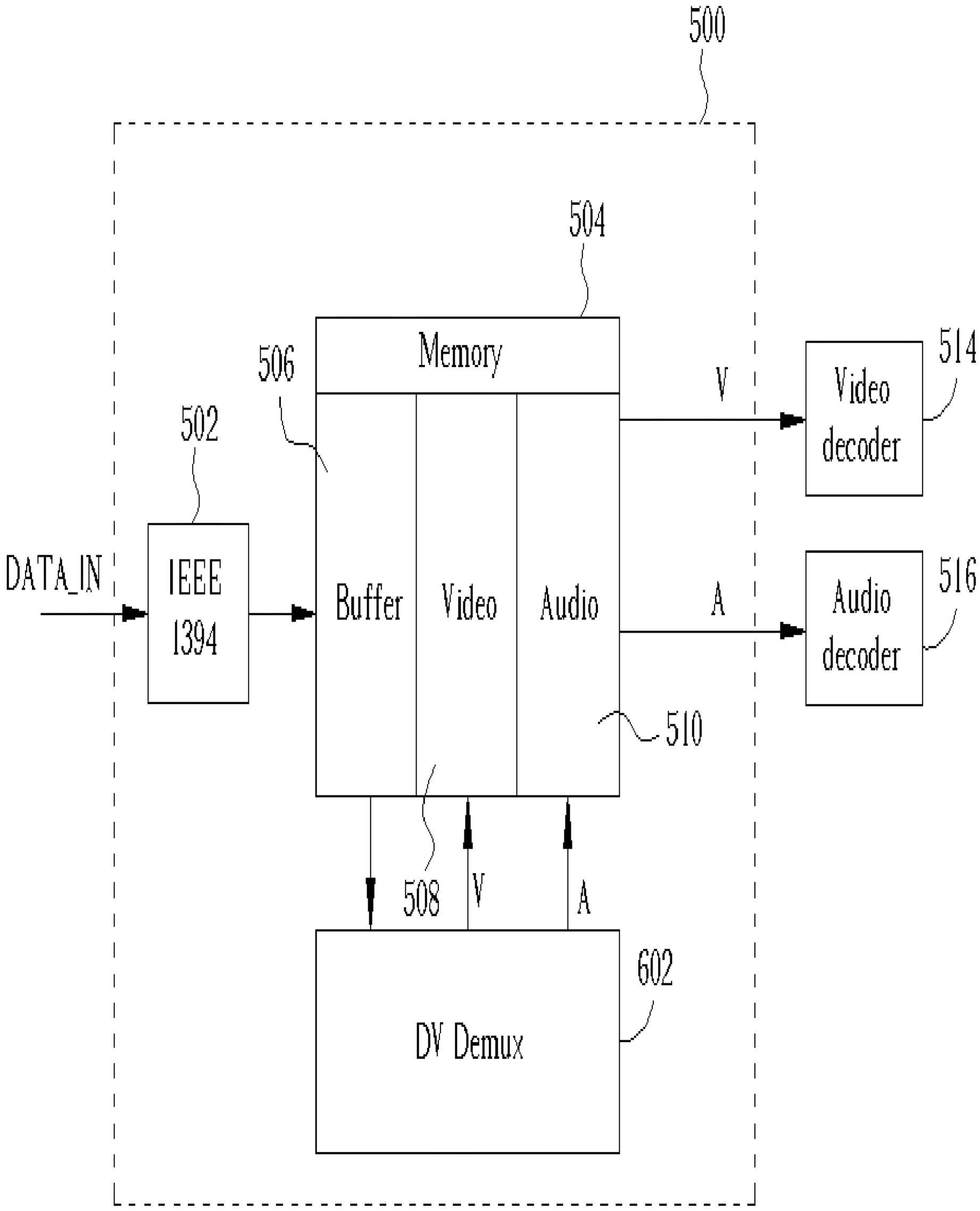

Fig. 6 Prior art

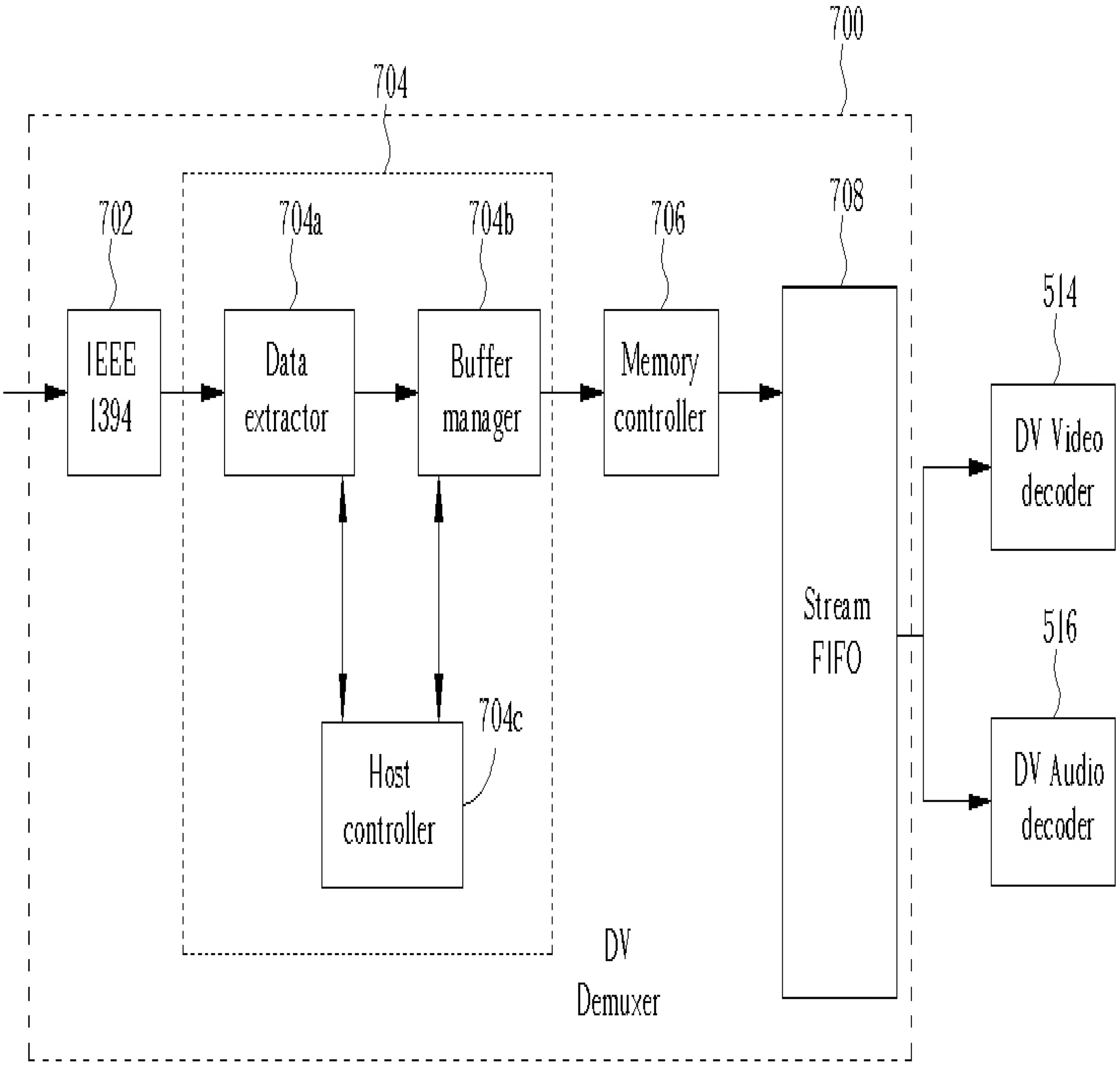
700
704
702
704a
704b
706
708
514
IEEE 1394
Data extractor
Buffer manager
Memory controller
DV Video decoder
Stream FIFO
516
704c
Host controller
DV Audio decoder
DV Demuxer

Fig. 7

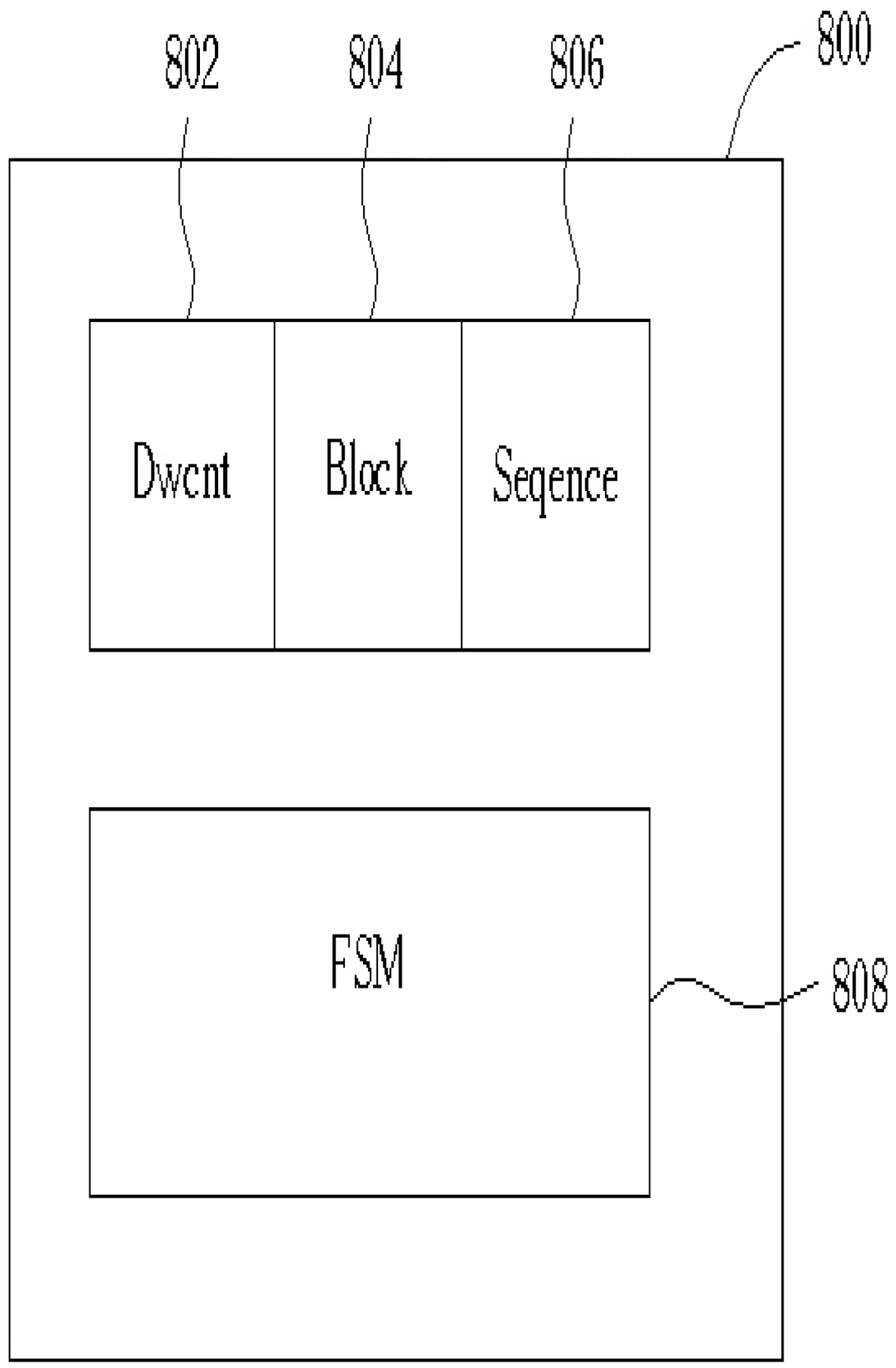

Fig. 8

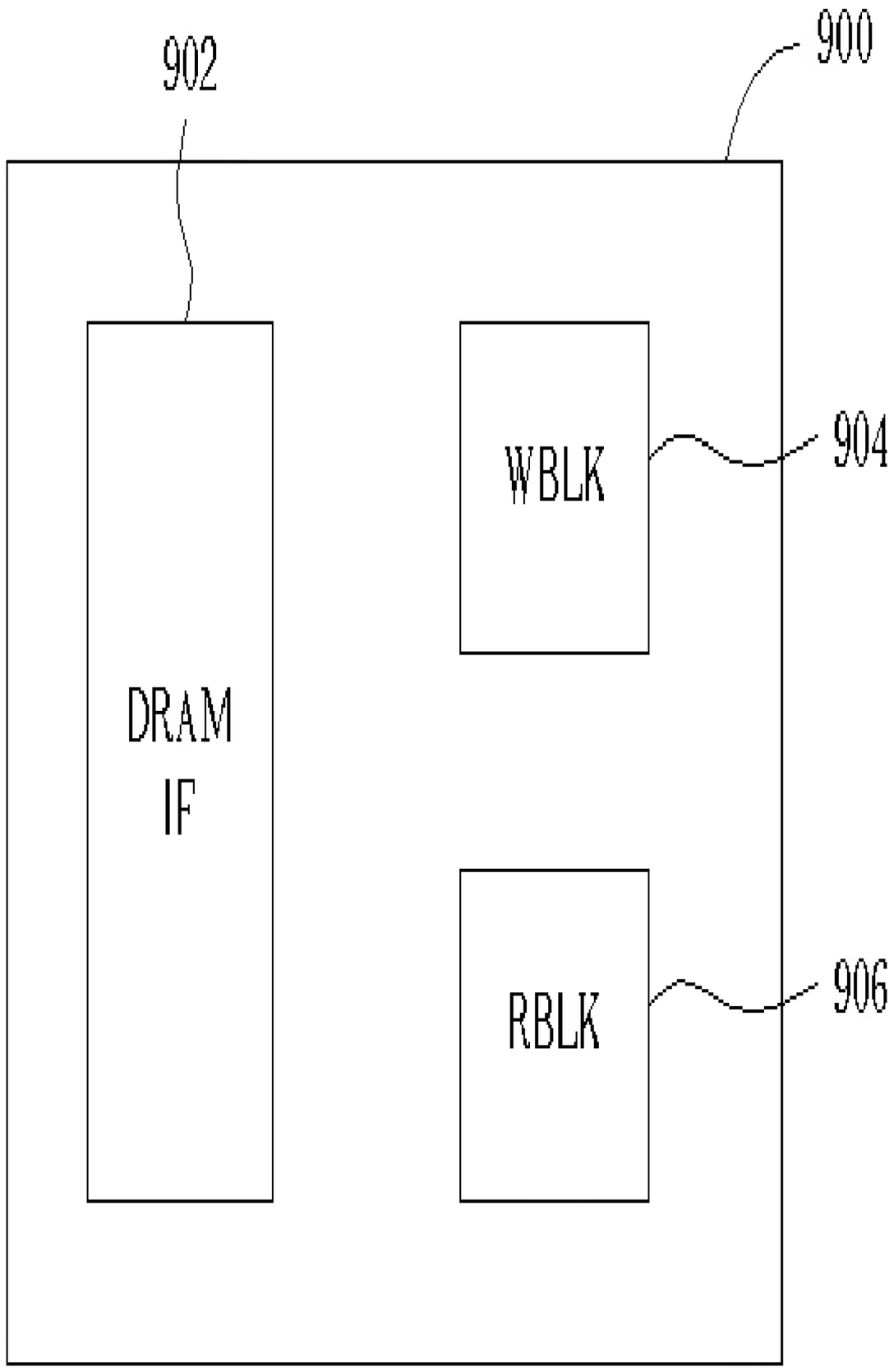

Fig. 9

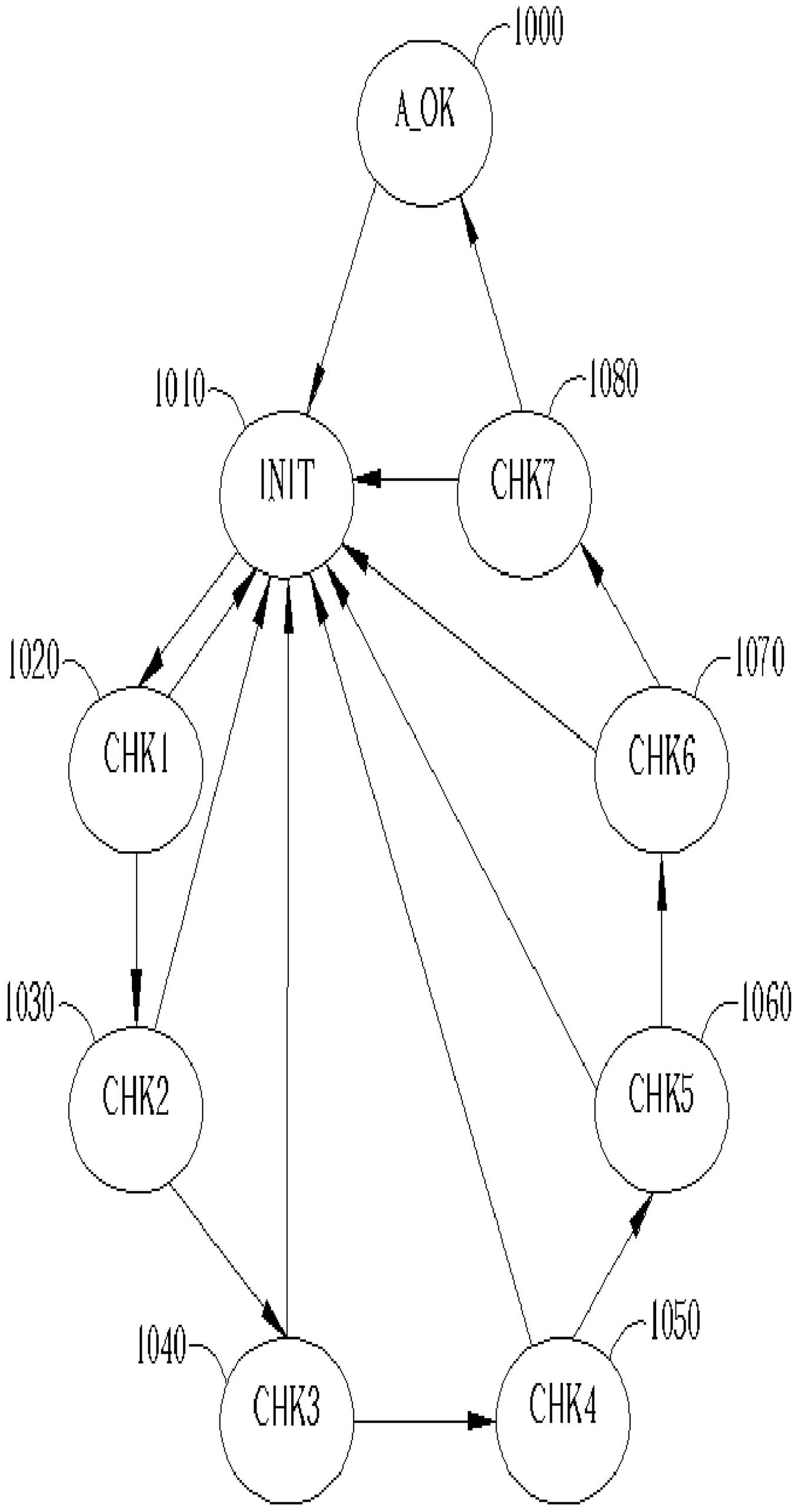
1000
A_OK
1010
INIT
1080
CHK7
1020
CHK1
1070
CHK6
1030
CHK2
1060
CHK5
1040
CHK3
1050
CHK4

Fig. 10

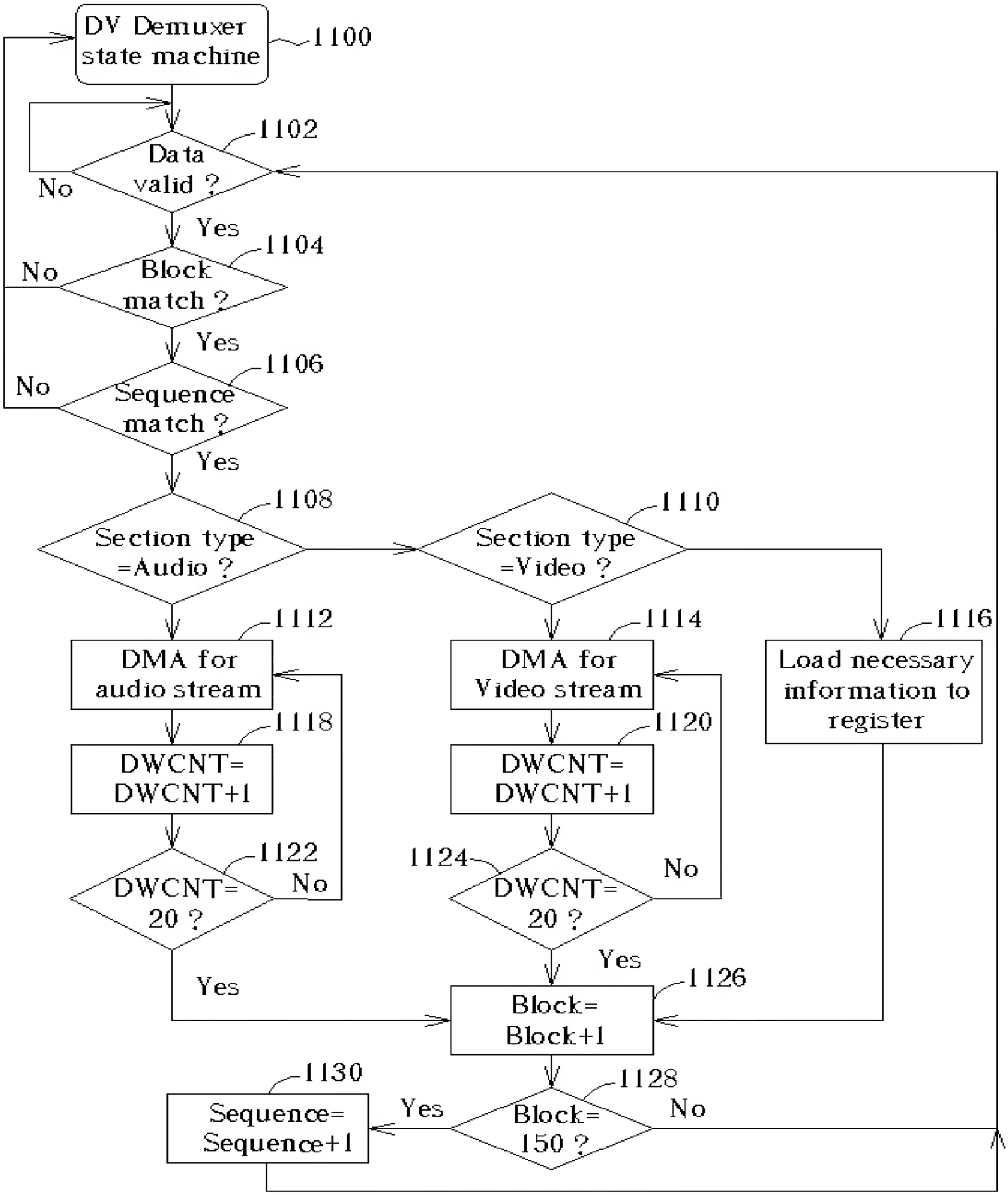
DV Demuxer state machine
1100
1102
Data valid ?
No
Yes
1104
Block match ?
No
Yes
1106
Sequence match ?
No
Yes
1108
Section type =Audio ?
1110
Section type =Video ?
1112
DMA for audio stream
1114
DMA for Video stream
1116
Load necessary information to register
1118
DWCNT= DWCNT+1
1120
DWCNT= DWCNT+1
1122
DWCNT= 20 ?
No
1124
DWCNT= 20 ?
No
Yes
1126
Block= Block+1
1128
Block= 150 ?
Yes
No
1130
Sequence= Sequence+1

Fig. 11

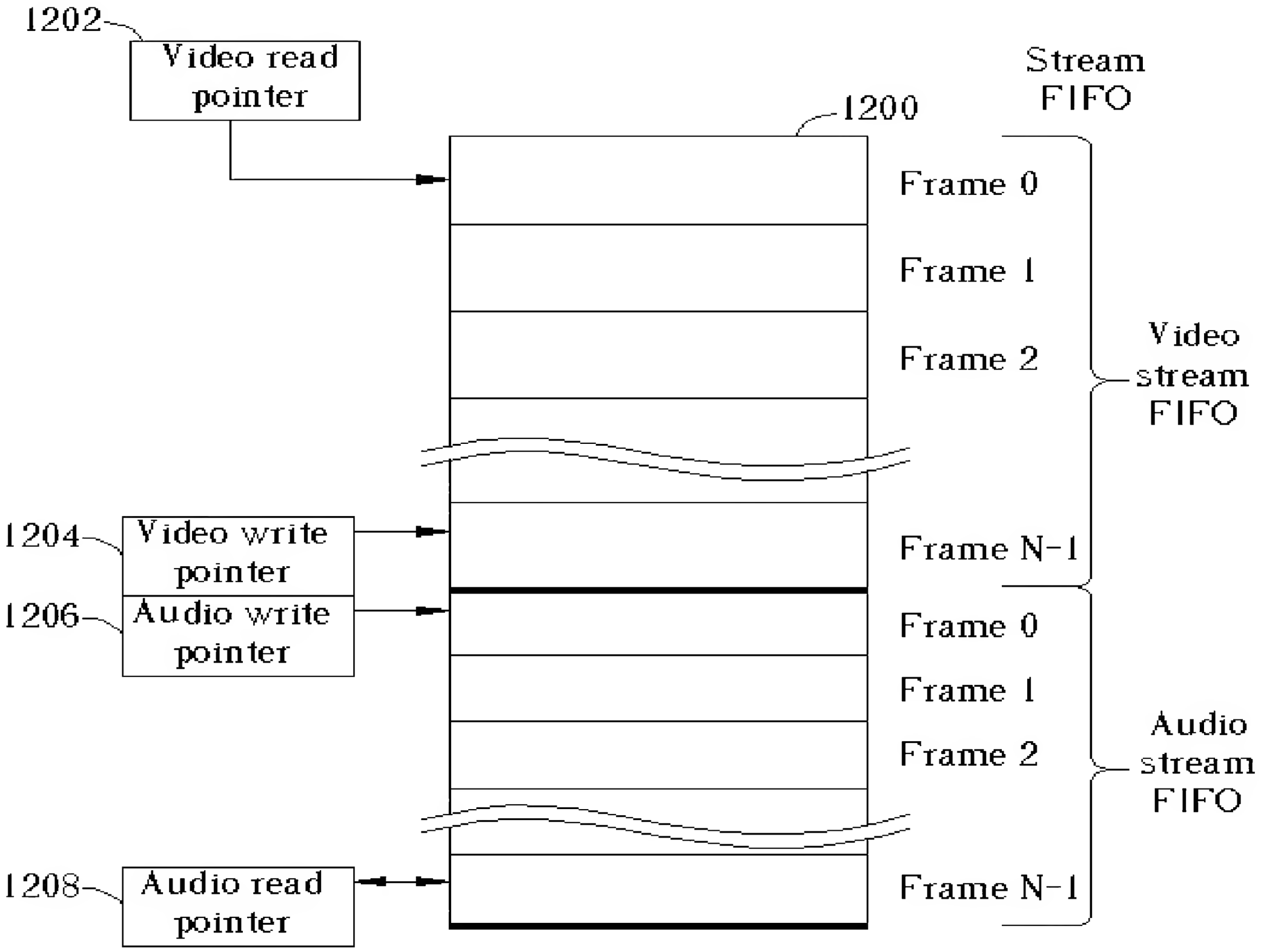
1202
Video read pointer
1200
Stream FIFO
Frame 0
Frame 1
Frame 2
Video stream FIFO
Frame N-1
1204
Video write pointer
1206
Audio write pointer
Frame 0
Frame 1
Frame 2
Audio stream FIFO
Frame N-1
1208
Audio read pointer

Fig. 12

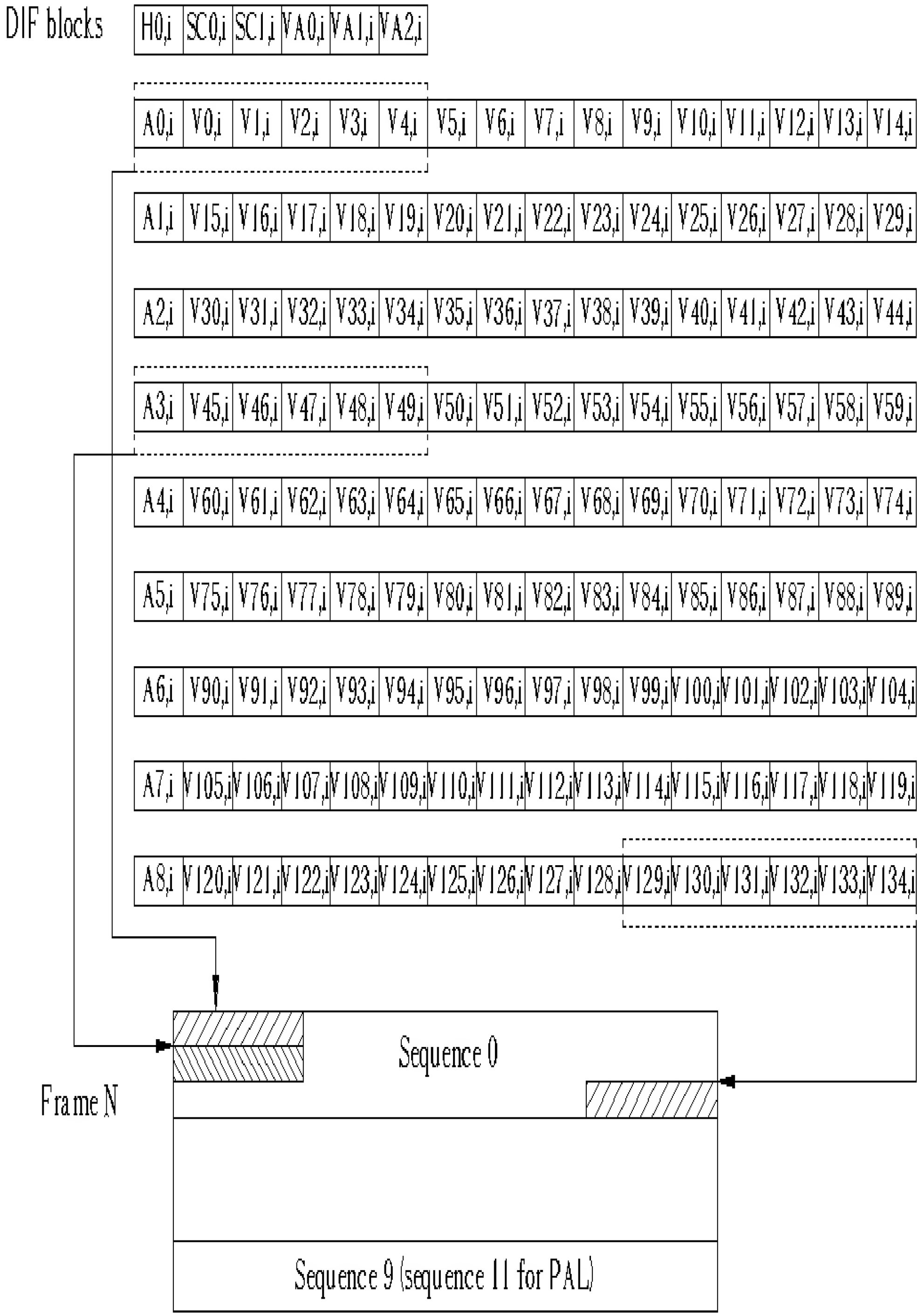
DIF blocks
H0,i SC0,i SC1,i VA0,i VA1,i VA2,i
A0,i V0,i V1,i V2,i V3,i V4,i V5,i V6,i V7,i V8,i V9,i V10,i V11,i V12,i V13,i V14,i
A1,i V15,i V16,i V17,i V18,i V19,i V20,i V21,i V22,i V23,i V24,i V25,i V26,i V27,i V28,i V29,i
A2,i V30,i V31,i V32,i V33,i V34,i V35,i V36,i V37,i V38,i V39,i V40,i V41,i V42,i V43,i V44,i
A3,i V45,i V46,i V47,i V48,i V49,i V50,i V51,i V52,i V53,i V54,i V55,i V56,i V57,i V58,i V59,i
A4,i V60,i V61,i V62,i V63,i V64,i V65,i V66,i V67,i V68,i V69,i V70,i V71,i V72,i V73,i V74,i
A5,i V75,i V76,i V77,i V78,i V79,i V80,i V81,i V82,i V83,i V84,i V85,i V86,i V87,i V88,i V89,i
A6,i V90,i V91,i V92,i V93,i V94,i V95,i V96,i V97,i V98,i V99,i V100,i V101,i V102,i V103,i V104,i
A7,i V105,i V106,i V107,i V108,i V109,i V110,i V111,i V112,i V113,i V114,i V115,i V116,i V117,i V118,i V119,i
A8,i V120,i V121,i V122,i V123,i V124,i V125,i V126,i V127,i V128,i V129,i V130,i V131,i V132,i V133,i V134,i
Sequence 0
Frame N
Sequence 9 (sequence 11 for PAL)

Fig. 13

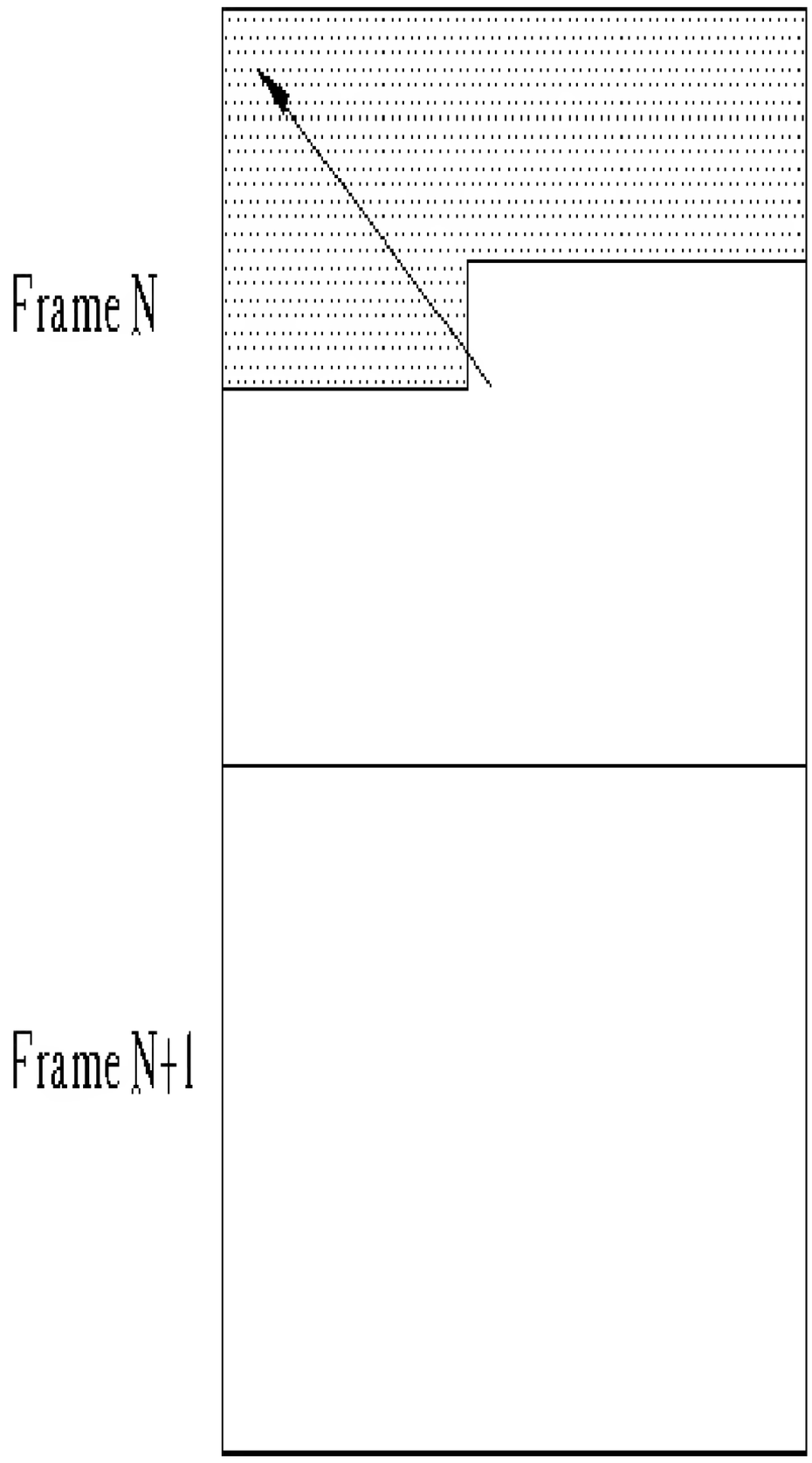

Fig. 14

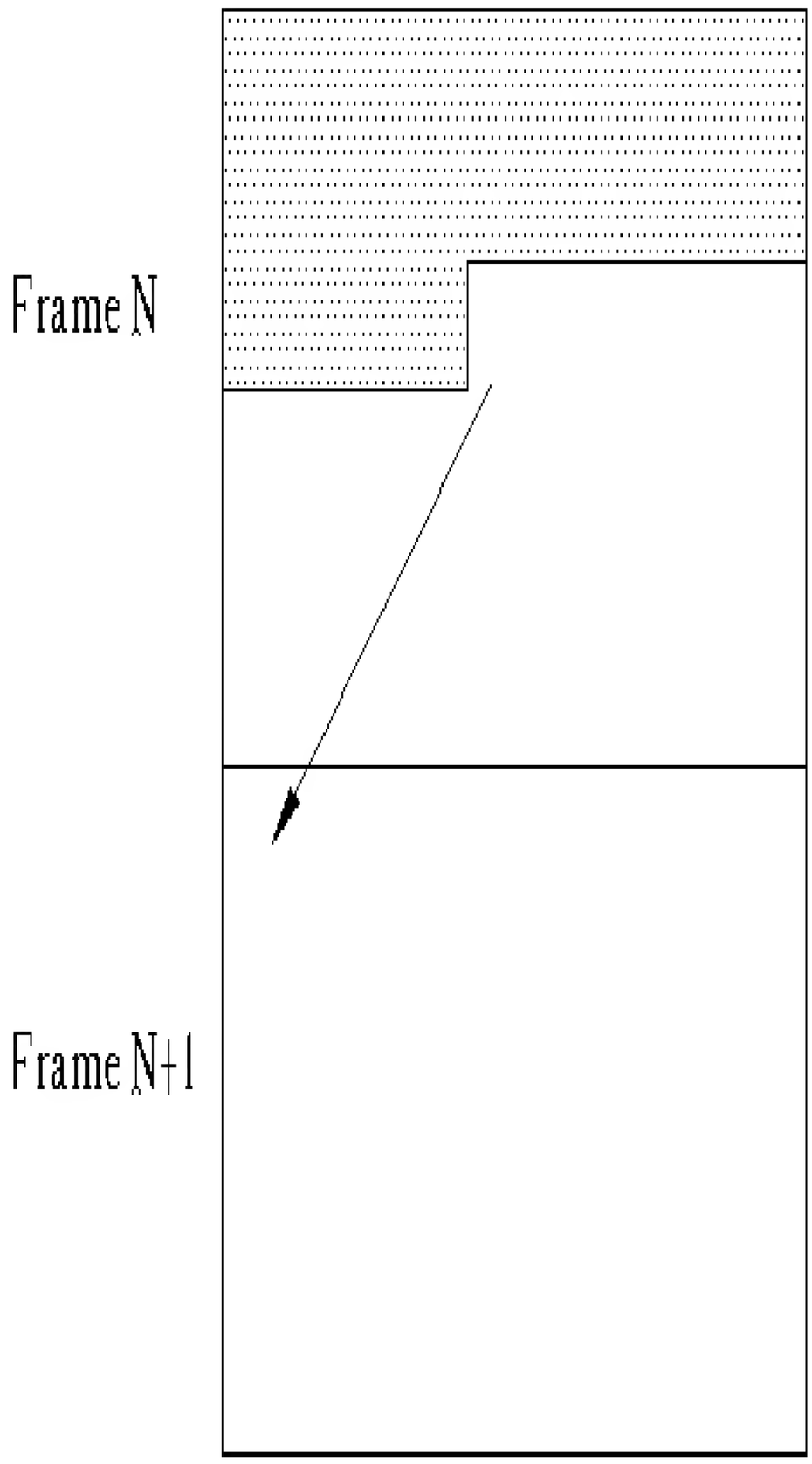

Fig. 15